AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0014] with the following amended paragraph:

[0014] In a preferred embodiment, the claimed invention provides a method of fabricating an interlayer dielectric layer of a low temperature polysilicon thin film transistor. First, a substrate with a polysilicon film is provided. Then, a gate insulating layer and a gate are formed on the polysilicon film in sequence. An ion implantation process is performed to form a source and a drain ~~surrounded the gate~~. After that, a first plasma enhanced chemical vapor deposition (PECVD) process is performed to form a silicon nitride layer over the substrate and the gate. A second plasma enhanced chemical vapor deposition process is then performed to form a TEOS based silicon oxide layer on the silicon nitride layer. A photo-etching process follows to form a contact hole on the source and another contact hole on the drain respectively. Then, a conductive layer is filled into the contact holes and electrically connected ~~to~~ with the source and drain.

Please replace paragraph [0020] with the following amended paragraph:

[0020] Please refer to Fig.5 to Fig.9, which are schematic diagrams of fabricating an interlayer dielectric layer of a low temperature polysilicon thin

film transistor according a first embodiment of the present invention. As mentioned above, though a display panel normally comprises a plurality of low temperature polysilicon thin film transistors, only one low temperature polysilicon thin film transistor is illustrated in the following diagrams for clarity. As shown in Fig. 5, a display panel 110 comprises a substrate 112 ~~on the surface thereof~~. The substrate 112 is a glass substrate or a silicon substrate. A chemical vapor deposition process or a sputtering process is performed to form an amorphous silicon film (not shown) with a thickness of 500 angstrom on ~~a display panel 110~~ the substrate 112. An excimer laser annealing (ELA) process follows to make the amorphous silicon film crystallize to a polysilicon film 114. Then, a first photo-etching process is performed to pattern the polysilicon film 114 and ~~leave~~ remain a predetermined portion for forming the low temperature polysilicon thin film transistors. The patterned polysilicon film 114 comprises a source region 118, a drain region 120, and a channel region 122 on the surface of the polysilicon film 114.

Please replace paragraph [0021] with the following amended paragraph:

[0021] As mentioned, since the quality of the amorphous silicon ~~thin~~ film (not shown) is a determining factor for the characteristics of the subsequently formed polysilicon layer 114, all of the parameters for the amorphous silicon ~~thin~~ film deposition process need to be strictly controlled. An amorphous silicon ~~thin~~

film with low hydrogen content, high thickness uniformity, and low surface roughness is thus formed. Moreover, the amorphous silicon ~~thin~~ film is melted and re-crystallized rapidly through absorption of deep ultraviolet light during the excimer laser annealing process to form the polysilicon layer 114. Such a quick absorption due to the short laser pulse only affects ~~the surface of~~ the amorphous silicon ~~thin~~ film and will not affect the substrate 112. Hence, the substrate 112 is kept at a low temperature state.

Please replace paragraph [0024] with the following amended paragraph:

[0024] As shown in Fig.8, a first plasma enhanced chemical vapor deposition (PECVD) process is performed by inputting silane (SiH4), ammonia (NH_3), and nitrogen (N_2) to form a silane based silicon nitride layer (SiN_x layer, $1.0<x<1.6$) 132 covering on the gate 126 and the gate insulating layer ~~234~~124. Then, a second PECVD process is performed by inputting tetra-ethyl-ortho-silicate (TEOS) and oxygen to form a tetra-ethyl-ortho-silicate based silicon oxide layer (TEOS-based SiO_x layer) 134 on the silicon nitride layer 132. The silane based silicon nitride layer 132 and the TEOS based silicon oxide layer 134 together form a composite interlayer dielectric layer.

Please replace paragraph [0025] with the following amended paragraph:

[0025] It is noted that since the dielectric constant

of the silicon nitride layer 132 is much higher than the dielectric constant of the silicon oxide layer 134, the present invention method can effectively avoid an overly high capacitance value in the composite interlayer dielectric layer, which leads to signal delay, by adjusting the thickness for the silicon oxide layer 134 to be greater than that of the silicon nitride layer 132. In a preferred embodiment of the present invention, a thickness of the silicon nitride layer 132 is in a range of 500 to ~~3500~~5000 angstroms and a thickness of the silicon oxide layer 134 is in a range of 500~~2500~~ to 10000 angstroms. In addition, the first PECVD process and the second PECVD process can be performed in ~~a single wafer type~~ the same chamber continuously or in different ~~single wafer type~~ chambers.

Please replace paragraph [0026] with the following amended paragraph:

[0026] As shown in Fig.9, a third photo-etching process is performed to form a contact hole 136 on the source region 118 and ~~another contact hole 136 on the~~ drain region 120 respectively. Then, a conductive layer 138 is filled into the contact holes 136 and electrically connected to the source 128 and the drain 130 ~~to~~ with complete the electrical connection of the low temperature polysilicon thin film transistor 131.

Please replace paragraph [0029] with the following amended paragraph:

[0029] Please refer to Fig.10 to Fig.12, which are schematic diagrams of fabricating an interlayer dielectric layer of a low temperature polysilicon thin film transistor according a second embodiment of the present invention. As shown in Fig.10, first, a gate 214 is directly formed on a substrate 212. Then, a gate insulating layer 216 and an amorphous silicon film 218 are formed on the gate 214 and the substrate 212 in sequence. Next, as shown in Fig.11, an excimer laser annealing process is performed to make the amorphous silicon film 218 melted and crystallize to a polysilicon film 220. An ion implantation process is performed thereafter to form a source 222 and a drain 224 in the polysilicon film 220 to form a bottom gate type of a low temperature polysilicon thin film transistor 226. As shown in Fig.12, in the same manner, a silane based silicon nitride layer 228 and a TEOS based silicon oxide layer 230 forms a composite interlayer dielectric layer 232 positioned on the low temperature polysilicon thin film transistor 226. Then, a contact hole 234 is formed on the source 222 and another contact hole 234 is formed on the drain 224. After that, a conductive layer 236 is filled into the contact holes 234 to complete the electrical connection of the low temperature polysilicon thin film transistor 226.